

<b>NOTICE OF REVISION (NOR)</b> (See MIL-STD-480 for instructions) This revision described below has been authorized for the document listed.		<b>DATE (YYMMDD)</b> 93-04-21	Form Approved OMB No. 0704-0188
Public reporting burden for this collection is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Washington, DC 20503.			
<b>1. ORIGINATOR NAME AND ADDRESS</b> Defense Electronics Supply Center Dayton, Ohio 45444-5270		<b>2. CAGE CODE</b> 67268	<b>3. NOR NO.</b> 5962-R142-93
		<b>4. CAGE CODE</b> 67268	<b>5. DOCUMENT NO.</b> 5962-87671
<b>6. TITLE OF DOCUMENT</b> MICROCIRCUIT, DIGITAL, MEMORY, BIPOLAR, PROGRAMMABLE LOGIC, MONOLITHIC SILICON		<b>7. REVISION LETTER</b> C (Current)	D (New)
		<b>8. ECP NO.</b> None	
<b>9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES</b> All			
<b>10. DESCRIPTION OF REVISION</b>  Sheet 1: Revisions ltr column; add "D". Revisions description column; add "Changes in accordance with NOR 5962-R142-93". Revisions date column; add "93-04-21". Revision level block; add "D". Rev blocks above sheet numbers 7 add "D"  Sheet 7: tPHZ for device 19 needs changed from 8 ns to 10 ns max Revision level block; add "D"			
<b>11. THIS SECTION FOR GOVERNMENT USE ONLY</b>			
a. CHECK ONE <input checked="" type="checkbox"/> EXISTING DOCUMENT SUPPLEMENTED BY THIS NOR MAY BE USED IN MANUFACTURE. <input type="checkbox"/> REVISED DOCUMENT MUST BE RECEIVED BEFORE MANUFACTURER MAY INCORPORATE THIS CHANGE. <input type="checkbox"/> CUSTODIAN OF MASTER DOCUMENT SHALL MAKE ABOVE REVISION AND FURNISH REVISED DOCUMENT TO:			
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ECS	SIGNATURE AND TITLE Michael Frye BRANCH CHIEF	DATE (YYMMDD) 93-04-21	
<b>12. ACTIVITY ACCOMPLISHING REVISION</b> DESC-ECS	REVISION COMPLETED (Signature) Kenneth Rice	DATE (YYMMDD) 93-04-21	

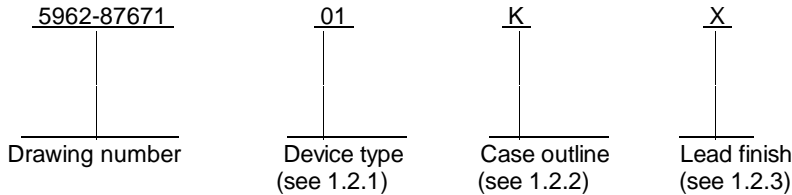
REVISIONS																				
LTR	DESCRIPTION										DATE (YR-MO-DA)	APPROVED								
A	Add vendor CAGE numbers 01295, 18324, and 34335 to the drawing. Added device types 05 and 06 for vendor CAGE number 34335. Change to absolute maximum ratings and table I. Editorial changes throughout.										90-03-29	M. Frye								
B	Add device types 11 through 18 for vendor CAGE 34335. Removed vendor CAGE 18324 as a source of supply for device types 05 and 06. Add vendor CAGE 01295 to device types 15 through 18, packages L, K, and 3. Editorial changes throughout.										91-05-09	M. Frye								
C	Changes to table I; conditions for I <sub>IH</sub> , limits on I <sub>CC</sub> , and limits on some timing conditions. Change pin 16 on case outline 3 to OE. Add device type 19. Editorial changes throughout.										93-02-19	M. Frye								
<p>THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.</p>																				
REV																				
SHEET																				
REV	C	C	C	C	C	C														
SHEET	15	16	17	18	19	20														
REV STATUS OF SHEETS				REV			C	C	C	C	C	C	C	C	C	C	C	C		
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14
PMIC N/A				PREPARED BY Kenneth Rice						DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444										
<b>STANDARDIZED MILITARY DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A				CHECKED BY Kenneth Rice																MICROCIRCUIT, DIGITAL, MEMORY, BIPOLAR, PROGRAMMING LOGIC, MONOLITHIC SILICON
				APPROVED BY Michael A. Frye																
				DRAWING APPROVAL DATE 87-09-20																
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										SHEET    1        OF        20										

## 1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	PAL20L8B	20-input 8-output AND-OR invert gate array
02	PAL20R8B	20-input 8-output registered AND-OR gate array
03	PAL20R6B	20-input 6-output registered AND-OR gate array
04	PAL20R4B	20-input 4-output registered AND-OR gate array
05	PLUS20L8	20-input 8-output AND-OR invert gate array
06	PLUS20R8	20-input 8-output registered AND-OR gate array
07	PAL20L8-15	20-input 8-output AND-OR invert gate array
08	PAL20R8-15	20-input 8-output registered AND-OR gate array
09	PAL20R6-15	20-input 6-output registered AND-OR gate array
10	PAL20R4-15	20-input 4-output registered AND-OR gate array
11	PAL20L8-12	20-input 8-output AND-OR invert gate array
12	PAL20R8-12	20-input 8-output registered AND-OR gate array
13	PAL20R6-12	20-input 6-output registered AND-OR gate array
14	PAL20R4-12	20-input 4-output registered AND-OR gate array
15	PAL20L8-10	20-input 8-output AND-OR invert gate array
16	PAL20R8-10	20-input 8-output registered AND-OR gate array
17	PAL20R6-10	20-input 6-output registered AND-OR gate array
18	PAL20R4-10	20-input 4-output registered AND-OR gate array
19	PAL20R8-7	20-input 8-output registered AND-OR gate array

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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### 1.3 Absolute maximum ratings.

Supply voltage range .....	-0.5 V dc to +7 V dc
Input voltage range .....	-1.5 V dc at -18 mA to +5.5 V
Storage temperature range .....	-65° C to +150° C
Lead temperature (soldering, 10 seconds) .....	+260° C
Thermal resistance, junction-to-case ( $\Theta_{JC}$ ) <sup>1/</sup> .....	See MIL-STD-1835
Output voltage applied .....	5.5 V dc
Output sink current .....	100 mA
Maximum power dissipation ( $P_D$ ) <sup>2/</sup> .....	1.2 W
Maximum junction temperature ( $T_J$ ) .....	+175° C

### 1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ) .....	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage ( $V_{IH}$ ) .....	2.0 V dc
Maximum low level input voltage ( $V_{IL}$ ) .....	0.8 V dc
Case operating temperature range ( $T_C$ ) .....	-55° C to +125° C

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

### SPECIFICATION

#### MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

### STANDARDS

#### MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
MIL-STD-1835 - Microcircuit Case Outlines.

### BULLETIN

#### MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

<sup>1/</sup> Heat sinking is recommended to reduce the junction temperature.

<sup>2/</sup> Must withstand the added  $P_D$  due to short circuit test (e.g.,  $I_{OS}$ ).

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### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered drawing.

3.2.4 Logic diagram. The logic diagram for unprogrammed devices shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical test for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55° C ≤ T <sub>C</sub> ≤ +125° C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA	1	All		-1.5	V
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IL</sub> ≤ 0.8 V, V <sub>IH</sub> ≥ 2.0 V, I <sub>OH</sub> = -2 mA	1, 2, 3	01-18	2.4		V
			1, 2	19	2.4		
			3	19	2.3		
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IL</sub> ≤ 0.8 V, V <sub>IH</sub> ≥ 2.0 V, I <sub>OL</sub> = 12 mA	1, 2, 3	All		0.5	V
High level input voltage	V <sub>IH</sub>	V <sub>CC</sub> = 5.5 V <u>2/</u>	1, 2, 3	All	2.0		V
Low level input voltage	V <sub>IL</sub>	V <sub>CC</sub> = 5.5 V <u>2/</u>	1, 2, 3	All		0.8	V
High level input current	I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.4 V, <u>3/</u> all other pins = 0.0 V	1, 2, 3	All		40	μA
						25	
Low level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V <u>3/</u>	1, 2, 3	All		-0.25	mA
Output short circuit current	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V <u>4/</u> V <sub>IH</sub> ≥ 2.0 V, V <sub>IL</sub> ≤ 0.8 V	1, 2, 3	01, 02, 03, 04, 07, 08, 09, 10, 11, 12, 13, 14, 15, 16, 17, 18	-30	-250	mA
				05, 06	-30	-90	
				19	-30	-130	
Input current	I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V	1, 2, 3	All		1.0	mA
Off-state output current	I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> ≤ 0.8 V V <sub>IH</sub> ≥ 2.0 V, V <sub>O</sub> = 0.4 V <u>3/</u>	1, 2, 3	All		-250	μA
Off-state output current	I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> ≤ 0.8 V V <sub>IH</sub> ≥ 2.0 V, V <sub>O</sub> = 2.4 V <u>3/</u>	1, 2, 3	All		100	μA
Supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V	1, 2, 3	01-14		210	mA
				15-19		220	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55° C ≤ T <sub>C</sub> ≤ +125° C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay data input to output	t <sub>PHL</sub>	V <sub>CC</sub> = 5.0 V, ±10 percent, C <sub>L</sub> = 50 pF R <sub>1</sub> = 390Ω, R <sub>2</sub> = 750Ω, or equivalent	9, 10, 11	01,03, 04		20	ns
				07,09, 10		15	
				11,13, 14		12	
				05,15, 17,18		10	
Propagation delay data input to output	t <sub>PLH</sub>		9, 10, 11	01,03, 04		20	ns
				07,09, 10		15	
				11,13, 14		12	
				05,15, 17,18		10	
Propagation delay high impedance to output high	t <sub>PZH</sub>		9, 10, 11	01,03, 04		25	ns
				07,09, 10,11, 13,14		15	
				05,15, 17,18		12	
Propagation delay high impedance to output low	t <sub>PZL</sub>		9, 10, 11	01,03, 04		25	ns
				07,09, 10,11, 13,14		15	
				05,15, 17,18		12	
Propagation delay output high to high impedance <sup>5/</sup>	t <sub>PHZ</sub>		9, 10, 11	01,03, 04		20	ns
				07,09, 10,11, 13,14		15	
				05,15, 17,18		12	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55° C ≤ T <sub>C</sub> ≤ +125° C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay output low to high impedance <u>5/</u>	t <sub>PLZ</sub>	V <sub>CC</sub> = 5.0 V, ±10 percent, C <sub>L</sub> = 50 pF R <sub>L</sub> = 390Ω, R <sub>2</sub> = 750Ω, or equivalent	9, 10, 11	01,03, 04		20	ns
				07,09, 10,11, 13,14		15	
				05,15, 17,18		12	
Propagation delay high impedance to output high (pin 13 to output enable)	t <sub>PZH</sub>		9, 10, 11	02,03, 04		20	ns
				08,09, 10,12, 13,14		15	
				06,16, 17,18		12	
Propagation delay high impedance to output low (pin 13 to output enable)	t <sub>PZL</sub>		9, 10, 11	19		8	ns
				02,03, 04		20	
				08,09, 10,12, 13,14		15	
Propagation delay output high to high impedance (pin 13 to output disable) <u>5/</u>	t <sub>PHZ</sub>		9, 10, 11	06,16, 17,18		12	ns
				19		8	
				02,03, 04		20	
Propagation delay output low to high impedance (pin 13 to output disable) <u>5/</u>	t <sub>PLZ</sub>		9, 10, 11	08,09, 10,12, 13,14		15	ns
				06,16, 17,18		12	
				19		10	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55° C ≤ T <sub>C</sub> ≤ +125° C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock to output	t <sub>PCH</sub>	V <sub>CC</sub> = 5.0 V, ±10 percent, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 390Ω, R <sub>2</sub> = 750Ω, or equivalent	9, 10, 11	02,03,04, 08,09,10, 19		15 7	ns
	t <sub>PCL</sub>			06,12, 13,14		12	
				16,17,18 19		10 7	
				Minimum clock pulse width (high)	t <sub>ph(CL)</sub>	9, 10, 11	
06,08,09, 10,12,13, 14	10						
16,17,18	8						
19	5						
Minimum clock pulse width (low)	t <sub>pl(CL)</sub>	9, 10, 11	02,03, 04,08, 09,10	12		ns	
			06,12, 13,14	10			
			16,17, 18	8			
			19	5			
Minimum setup time <u>2/</u>	t <sub>su</sub>	9, 10, 11	02,03, 04	20		ns	
			08,09, 10	15			
			12,13, 14	12			
			16,17, 18	10			
			19	7			
Minimum hold time <u>2/</u>	t <sub>H</sub>		9, 10, 11	02,03, 04,08, 09,10, 12,13, 14,16, 17,18, 19	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Maximum clock frequency <sup>2/</sup> <sup>6/</sup>	f <sub>MAX</sub>	V <sub>CC</sub> = 5.0 V, ±10 percent, C <sub>L</sub> = 50 pF R <sub>L</sub> = 390Ω, R <sub>2</sub> = 750Ω, or equivalent	9, 10, 11	02,03, 04	41.6		MHz
				08,09, 10,12, 13,14,	50		
				16,17, 18	62.5		
				19	100		

1/ All voltages are referenced to ground.

2/ Tested only initially and after any design change.

3/ I/O terminal leakage is the worst case of I<sub>IX</sub> or I<sub>OZX</sub>.

4/ Only one output shorted at a time.

5/ C<sub>L</sub> = 5 pF. Equivalent testing may be used to simulate the 5 pF load.

6/ f<sub>MAX</sub> =  $\frac{1}{2 \times t_p(C_L)}$ .

$$2 \times \boxed{t_p(C_L)}$$

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T<sub>A</sub> = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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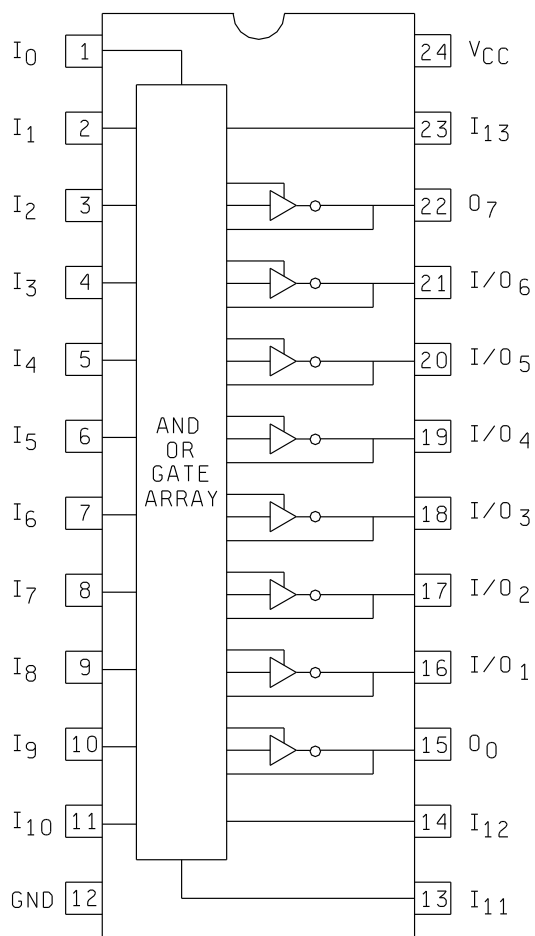
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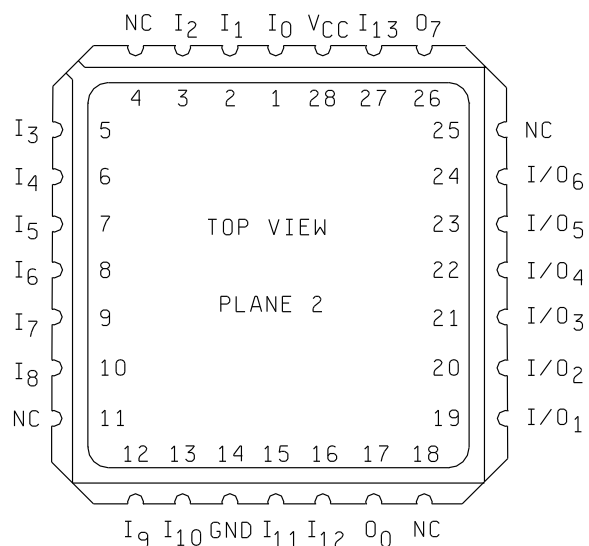
Device types 01, 05, 07, 11, and 15

CASE K and L



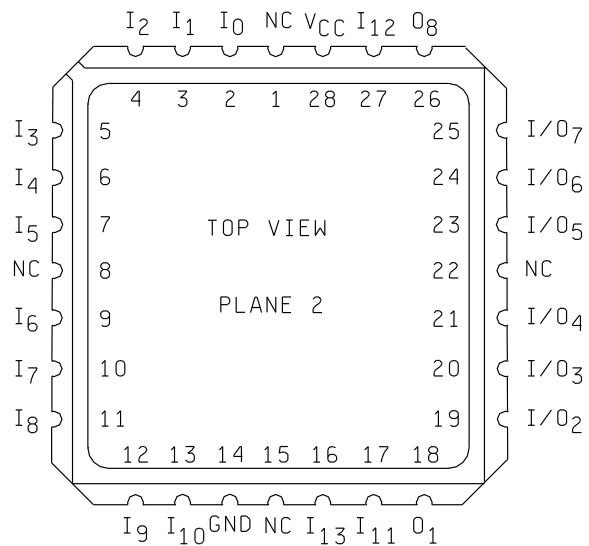
Device types 01 and 05

CASE 3



Device types 07, 11, and 15

CASE 3



NOTE: Previously on revision A of this document, device 07 was erroneously shown with the incorrect terminal connection for case 3 package.

FIGURE 1. Terminal connections.

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SIZE  
**A**

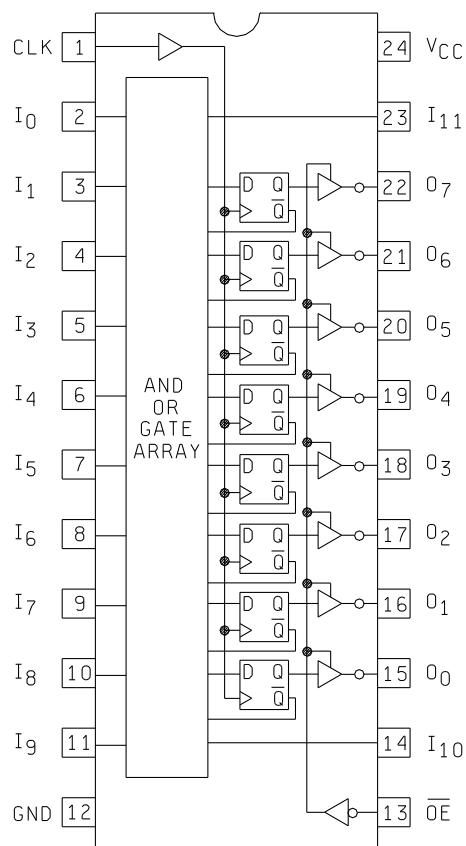
REVISION LEVEL  
**C**

**5962-87671**

SHEET  
**10**

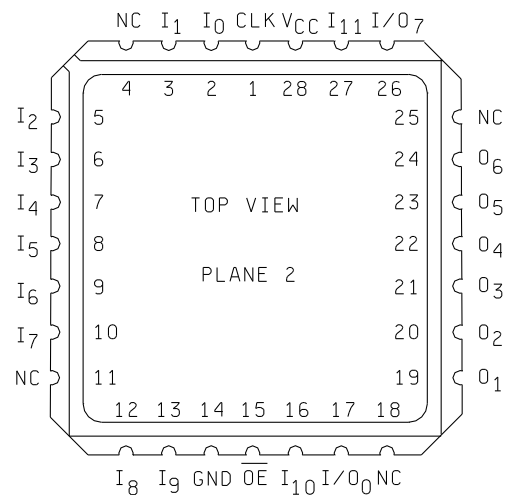
Device types 02, 06, 08, 16, and 19

CASE K and L



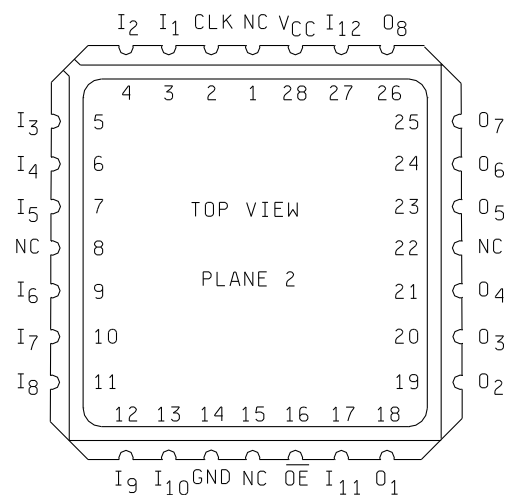
Device types 02 and 06

CASE 3



Device types 08, 12, 16, and 19

CASE 3



NOTE: Previously on revision A of this document, device 08 was erroneously shown with the incorrect terminal connection for case 3 package.

FIGURE 1. Terminal connections - Continued.

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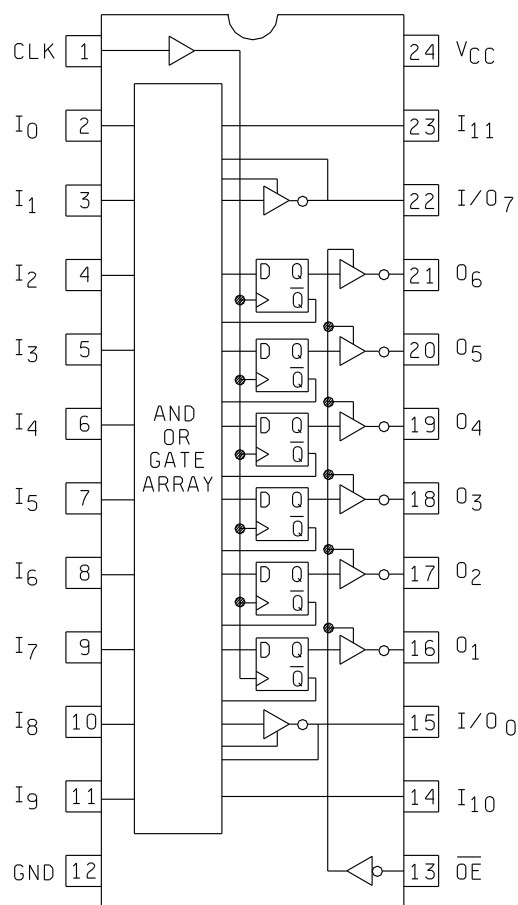
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**C**

SHEET  
**11**

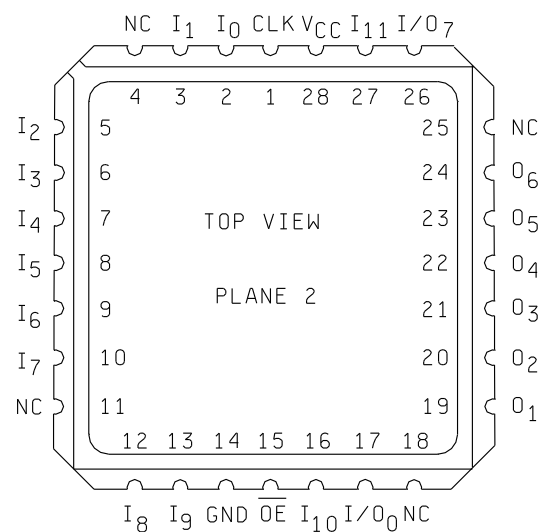
Device types 03, 09, 13, and 17

CASE K and L



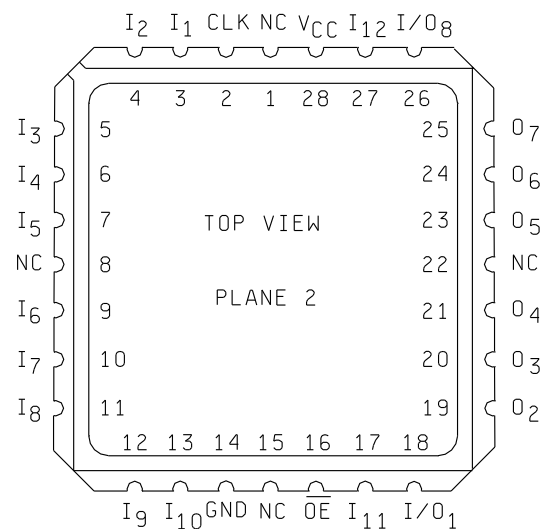
Device type 03

CASE 3



Device types 09, 13, and 17

CASE 3



NOTE: Previously on revision A of this document, device 09 was erroneously shown with the incorrect terminal connection for case 3 package.

FIGURE 1. Terminal connections - Continued.

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**A**

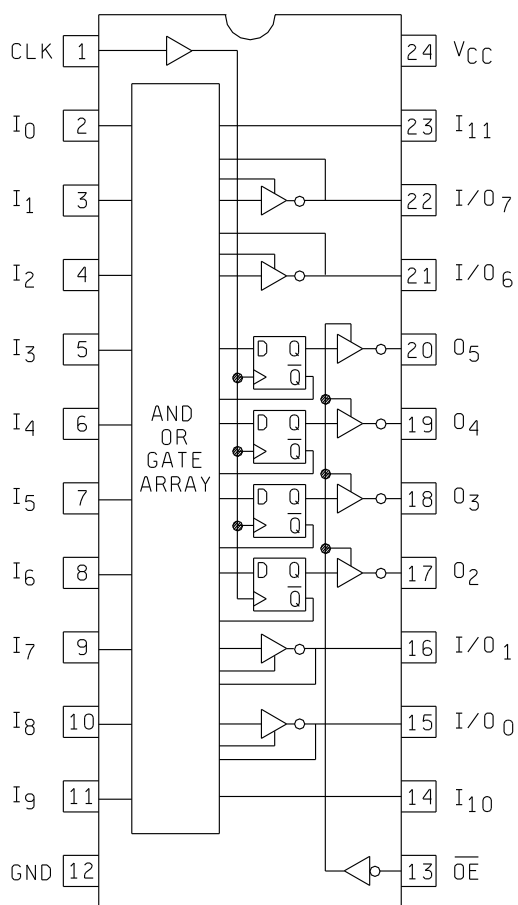
REVISION LEVEL  
C

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SHEET  
**12**

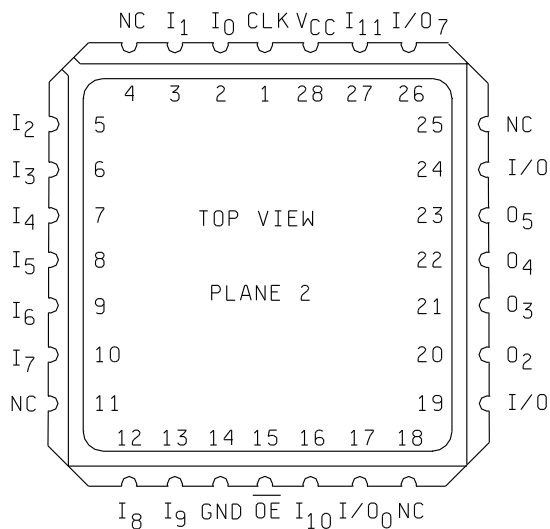
Device types 04, 10, 14, and 18

CASE K and L



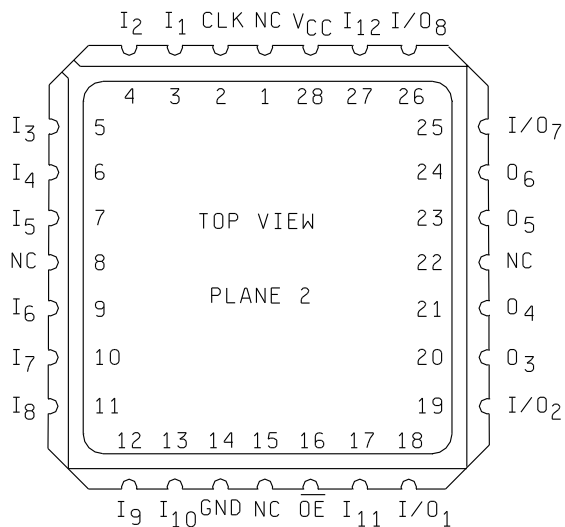
Device type 04

CASE 3



Device types 10, 14, and 18

CASE 3



NOTE: Previously on revision A of this document, device 10 was erroneously shown with the incorrect terminal connection for case 3 package.

FIGURE 1. Terminal connections - Continued.

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SHEET  
**13**

Device types 01, 05, 07, 11, 15

Inputs														Outputs						
I <sub>13</sub>	I <sub>12</sub>	I <sub>11</sub>	I <sub>10</sub>	I <sub>9</sub>	I <sub>8</sub>	I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	I/O <sub>6</sub>	I/O <sub>5</sub>	I/O <sub>4</sub>	I/O <sub>3</sub>	I/O <sub>2</sub>	I/O <sub>1</sub>	O <sub>0</sub>
X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z

Device types 02, 06, 08, 12, 16, 19

Inputs													Outputs								
OE	I <sub>11</sub>	I <sub>10</sub>	I <sub>9</sub>	I <sub>8</sub>	I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	CLK	O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	H	H	H	H	H	H	H	H

Device types 03, 09, 13, 17

Inputs													Outputs								
OE	I <sub>11</sub>	I <sub>10</sub>	I <sub>9</sub>	I <sub>8</sub>	I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	CLK	I/O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	I/O <sub>0</sub>
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	H	H	H	H	H	H	Z

Device types 04, 10, 14, 18

Inputs													Outputs								
OE	I <sub>11</sub>	I <sub>10</sub>	I <sub>9</sub>	I <sub>8</sub>	I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	CLK	I/O <sub>7</sub>	I/O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	I/O <sub>1</sub>	I/O <sub>0</sub>
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	H	H	H	H	Z	Z

FIGURE 2. Truth tables (unprogrammed).

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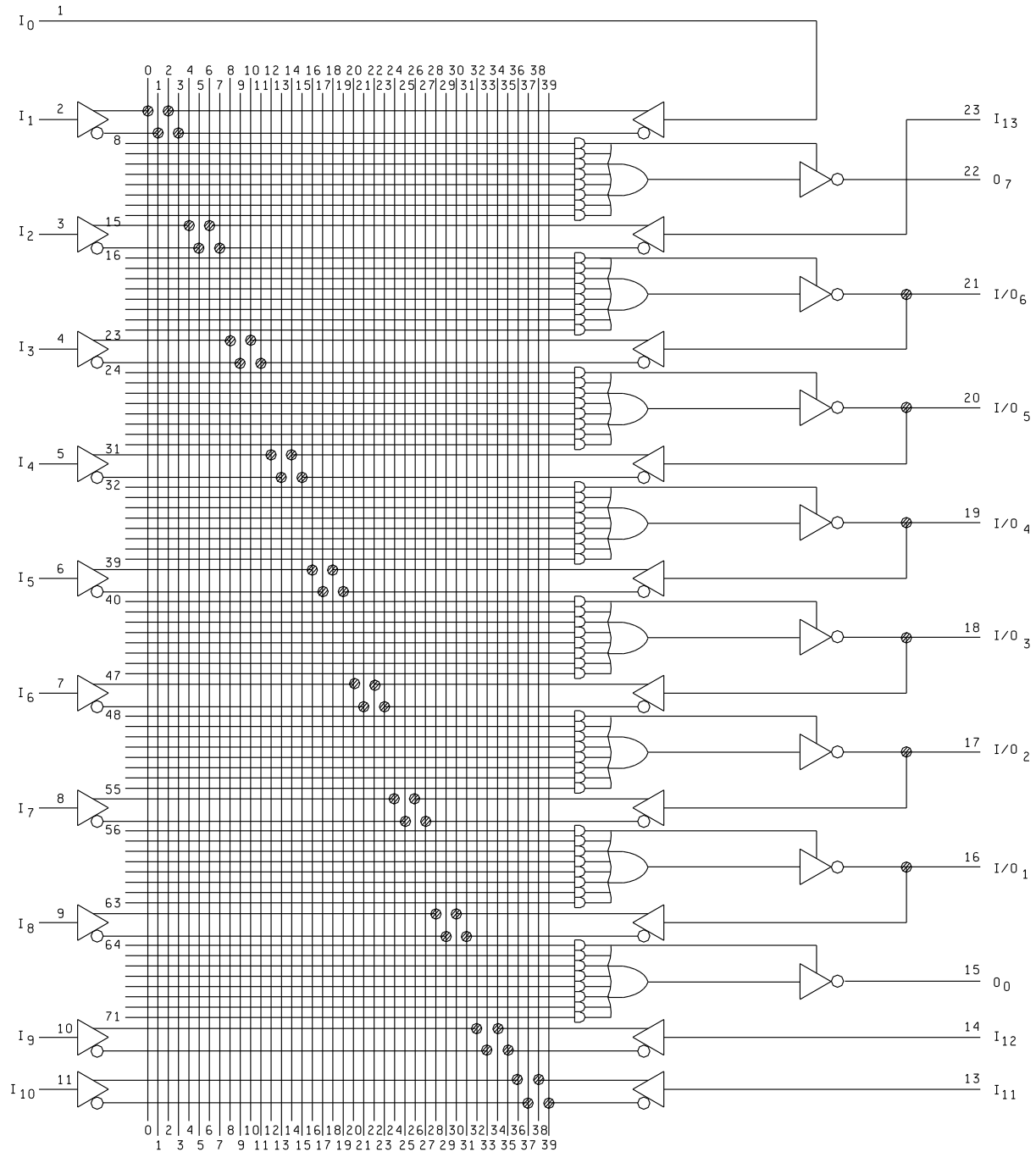


FIGURE 3. Unprogrammed logic diagrams.

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Device types 02, 06, 08, 12, 16, 19

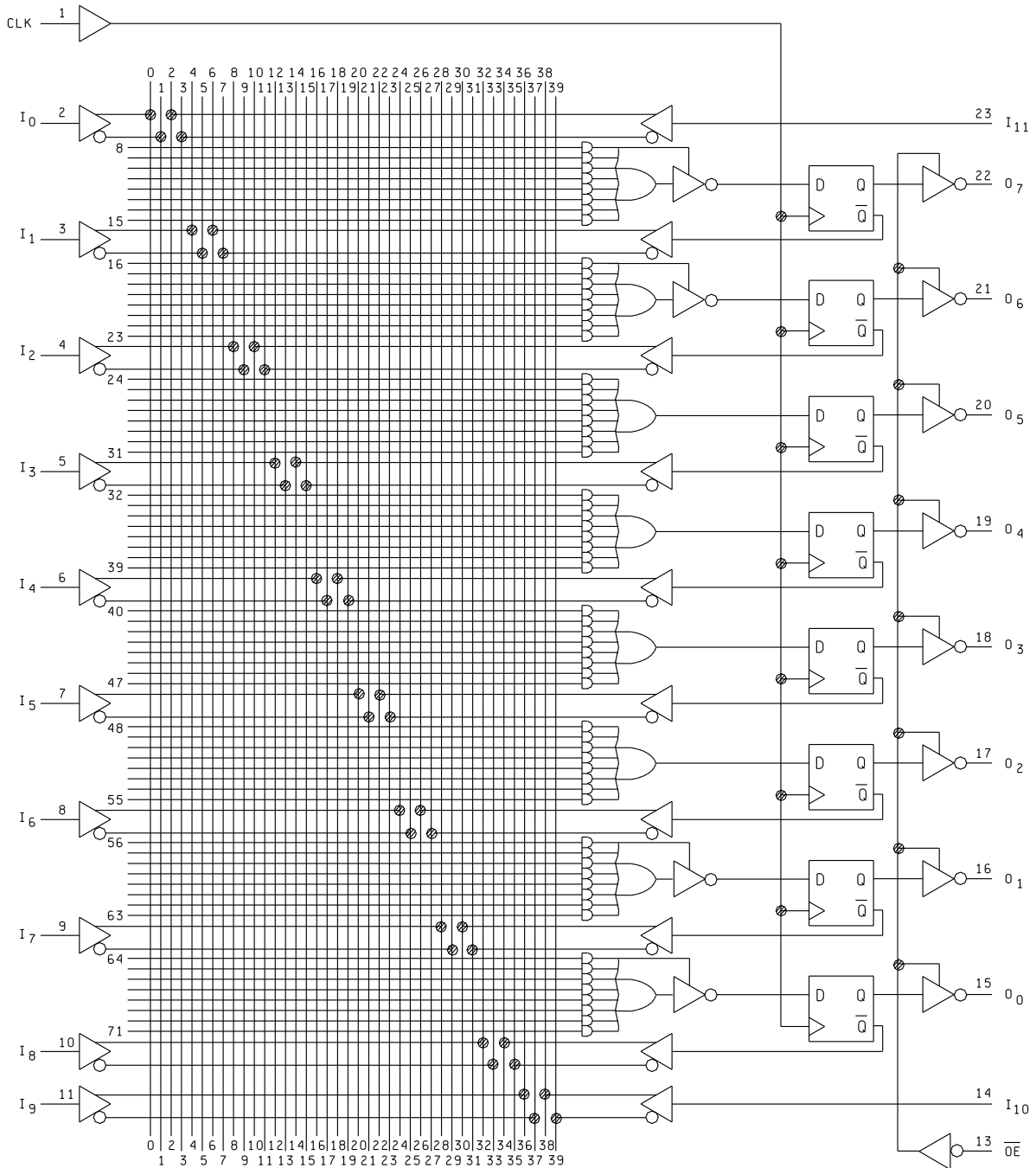


FIGURE 3. Unprogrammed logic diagrams - Continued.

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Device types 03, 09, 13, and 17

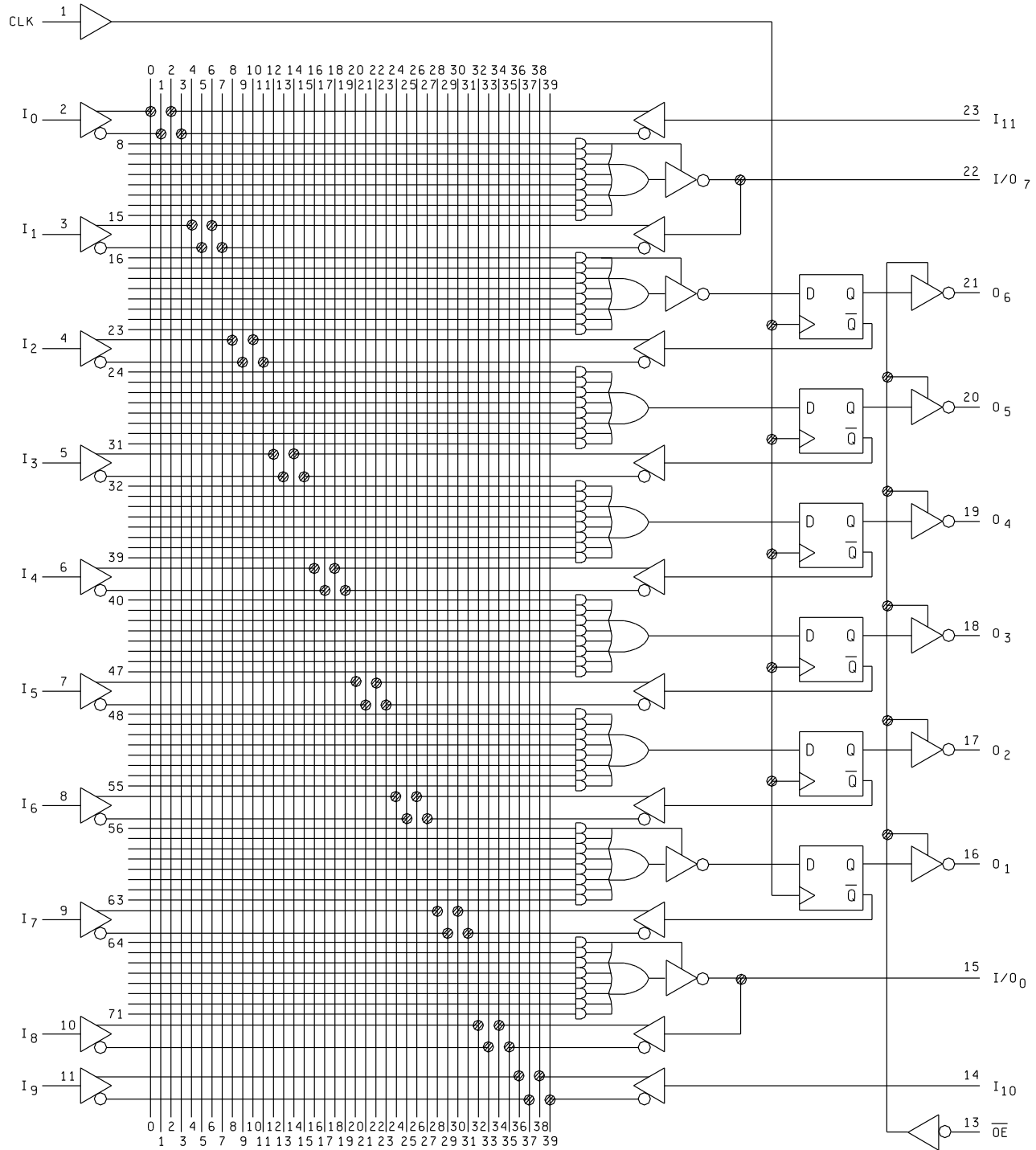


FIGURE 3. Unprogrammed logic diagrams - Continued.

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Device types 04, 10, 14, and 18

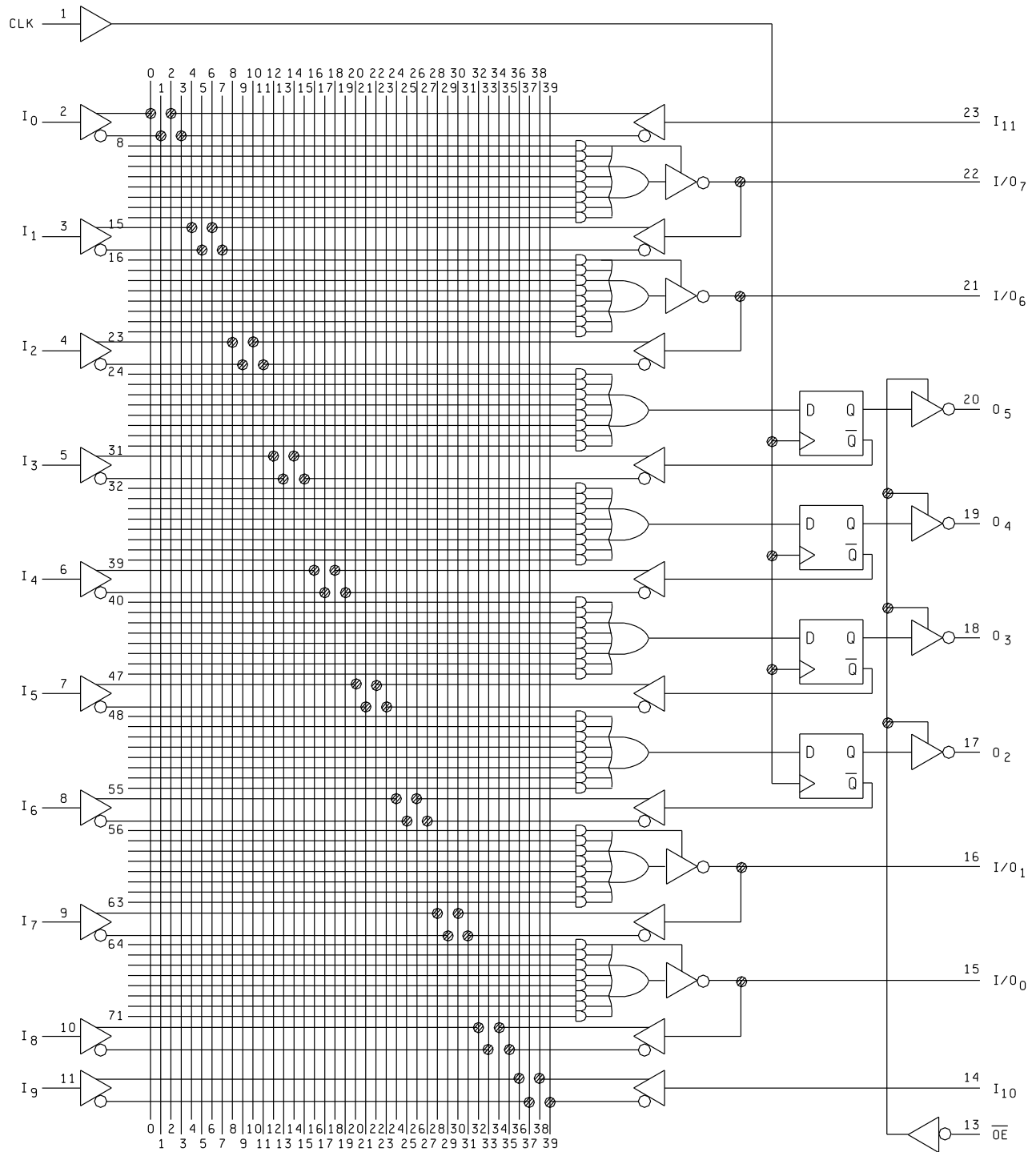


FIGURE 3. Unprogrammed logic diagrams - Continued.

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TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

1/ \* PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall also verify the truth table of figure 2 for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Unprogrammed devices, shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable.
  - (1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.
  - (2) If each compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1) If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If no more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.
- d. Subgroups 7 and 8 shall include verification of the truth table.

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#### 4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

#### 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

#### 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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## STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-02-19

Approved sources of supply for SMD 5962-87671 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1</u> /
5962-8767101KX	01295	TIBPAL20L8-20MWB
	50364	PAL20L8BMW/883B
5962-8767101LX	01295	TIBPAL20L8-20MJTB
	50364	PAL20L8BMJS/883B
5962-87671013X	01295	TIBPAL20L8-20MFDB
	50364	PAL20L8BML/883B
5962-8767102KX	01295	TIBPAL20R8-20MWB
	50364	PAL20R8BMW/883B
5962-8767102LX	01295	TIBPAL20R8-20MJTB
	50364	PAL20R8BMJS/883B
5962-87671023X	01295	TIBPAL20R8-20MFDB
	50364	PAL20R8BML/883B
5962-8767103KX	01295	TIBPAL20R6-20MWB
	50364	PAL20R6BMW/883B
5962-8767103LX	01295	TIBPAL20R6-20MJTB
	50364	PAL20R6BMJS/883B
5962-87671033X	01295	TIBPAL20R6-20MFDB
	50364	PAL20R6BML/883B
5962-8767104KX	01295	TIBPAL20R4-20MWB
	50364	PAL20R4BMW/883B
5962-8767104LX	01295	TIBPAL20R4-20MJTB
	50364	PAL20R4BMJS/883B
5962-87671043X	01295	TIBPAL20R4-20MFDB
	50364	PAL20R4BML/883B
5962-8767105KX	<u>2</u> /	PLUS20LB/BJA
5962-8767105LX	<u>2</u> /	PLUS20L8/BLA
5962-87671053X	<u>2</u> /	PLUS20LB/B3A

See footnotes at end of table.

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.

## STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN - Continued.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1</u> /
5962-8767106KX	<u>2</u> /	PLUS20R8/BKA
5962-8767106LX	<u>2</u> /	PLUS20RB/BLA
5962-87671063X	<u>2</u> /	PLUS20R8/B3A
5962-8767107LX	34335	PAL20L8-15/BLA
5962-87671073X	34335	PAL20L8-15B3A
5962-8767108LX	34335	PAL20R8-15/BLA
5962-87671083X	34335	PAL20R8-15/B3A
5962-8767109LX	34335	PAL20R6-15/BLA
5962-87671093X	34335	PAL20R6-15/B3A
5962-8767110LX	34335	PAL20R4-15/BLA
5962-87671103X	34335	PAL20L4-15/B3A
5962-8767111LX	34335	PAL20L8-12/BLA
5962-87671113X	34335	PAL20L8-12/B3A
5962-8767112LX	34335	PAL20R8-12/BLA
5962-87671123X	34335	PAL20R8-12/B3A
5962-8767113LX	34335	PAL20R6-12/BLA
5962-87671133X	34335	PAL20R6-12/B3A
5962-8767114LX	34335	PAL20R4-12/BLA
5962-87671143X	34335	PAL20R4-12/B3A
5962-8767115KX	01295	TIBPAL20L8-10MWB
5962-8767115LX	01295	TIBPAL20L8-10MJTB
	34335	PAL20L8-10/BLA
5962-87671153X	01295	TIBPAL20L8-10MFKB
	34335	PAL20L8-10/B3A
5962-8767116KX	01295	TIBPAL20R8-10MWB
5962-8767116LX	01295	TIBPAL20R8-10MJTB
	34335	PAL20R8-10/BLA
5962-87671163X	01295	TIBPAL20R8-10MFKB
	34335	PAL20R8-10/B3A
5962-8767117KX	01295	TIBPAL20R6-10MWB
5962-8767117LX	01295	TIBPAL20R6-10MJTB
	34335	PAL20R6-10/BLA
5962-87671173X	01295	TIBPAL20R6-10MFKB
	34335	PAL20R6-10/B3A

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN - Continued.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-8767118KX	01295	TIBPAL20R4-10MWB
5962-8767118LX	01295	TIBPAL20R4-10MJTB
	34335	PAL20R4-10/BLA
5962-87671183X	34335	PAL20R4-10/B3A
	01295	TIBPAL20R4-10MFKB
5962-8767119KX	01295	TIBPAL20R8-7MWB
5962-8767119LX	01295	TIBPAL20R8-7MJTB
5962-87671193X	01295	TIBPAL20R8-7MFKB

1/ Caution. Do not use this number for item acquisition.  
Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>	<u>Fusible-link</u>
01295	Texas Instruments, Incorporated 13500 N. Central Expressway P.O. Box 655305 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448	Titanium-tungsten
34335	Advance Micro Devices 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088	Titanium-tungsten
50364	MMI/AMD 2175 Mission College Boulevard Santa Clara, CA 95054-1592 Point of contact: 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088	Titanium-tungsten